WE CLAIM:

1. A method of fabricating a MIS transistor including a gate electrode forming step of forming a gate electrode containing polycrystalline silicon being opposed to a silicon substrate through a gate insulating film, a side wall forming step of forming side walls on both sides of said gate electrode, and a salicide step of forming desired silicide films on upper portions of said gate electrode and a source/drain layer,

said side wall forming step having steps of:

depositing a first insulating film on a region including at least one of said both sides of said gate electrode and a surface of said silicon substrate being allowed to be exposed by said gate electrode and in contact with said at least one of said both sides,

depositing a second insulating film being opposed to said at least one of said both sides and said surface through said first insulating film, and

etching back said first and second insulating films thereby forming said at least one of said both sides walls of a two-layer structure,

said method further including an etching step of etching said first insulating film in a larger amount than said second insulating film before said salicide step.

2. The method of fabricating a MIS transistor in accordance with claim 1, wherein compositions of said first and second insulating films are different from each other, said etching step being adapted to isotropically etch said first insulating film.

3. The method of fabricating a MIS transistor in accordance with claim 2, further including a step of roughening an upper surface of said gate electrode before said salicide step.

4. The method of fabricating a MIS transistor in accordance with claim 1, wherein compositions of said first and second insulating films are different from each other, said etching step being adapted to etch said first insulating film through anisotropic etching at a higher etching rate in a vertical direction being perpendicular to said silicon substrate as compared with an etching rate in a horizontal width direction.

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5. The method of fabricating a MIS transistor in accordance with claim 4, further including a step of roughening an upper surface of said gate electrode before said salicide step.

6. A MIS transistor including:

a gate electrode being formed to be opposed to a silicon substrate through a gate insulating film and having a silicified upper portion; and

side walls being formed on said silicon substrate on both sides of said gate electrode and having grooves being adjacent to said gate electrode,

said gate electrode being silicified up to walls of said gate electrode in said grooves.

7. The MIS transistor in accordance with claim 6, wherein a surface of said gate electrode is roughened.

8. The MIS transistor in accordance with claim 6, wherein said side walls have cavities exposing a source/drain layer being formed on said silicon substrate.

9. The MIS transistor in accordance with claim 8, wherein a surface of said gate electrode is roughened.

10. A MIS transistor including:

a gate electrode being formed to be opposed to a silicon substrate through a gate insulating film and having a silicified upper portion; and

side walls being formed on said silicon substrate on both sides of said gate electrode, said side walls being higher than said gate electrode,

said side walls being provided with silicon films on walls closer to said gate electrode to be connected with said gate electrode, a surface of said gate electrode being silicified up to surfaces of said silicon films.

11. The MIS transistor in accordance with claim 10, wherein both of said surfaces of said gate electrode and said silicon films are roughened.

12. A MIS transistor including:

a gate electrode being formed to be opposed to a silicon substrate through a gate insulating film and having a silicified upper portion; and

side walls having L-shaped sections being formed on said silicon substrate on both sides of said gate electrode, said side walls being higher than said gate electrode.

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13. The MIS transistor in accordance with claim 12, wherein a surface of said gate electrode is roughened.